# MODELING THE SCHOTTKY BARRIER PROPERTIES OF GRAPHENE NANORIBBON SCHOTTKY DIODE

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Dedicated to my beloved family.

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# ABSTRACT

The increasing demand for small sized, low power consumption and high processing speeds have always been the pillars of transistor development. To meet the demands of the transistor, the current trend is to reduce the size of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) into nanoscale regime because size plays an essential role in the performance of transistors. However, the extreme scaling of the size has brought new challenges as the MOSFET reaches its performance limit. In this respect, the Graphene Nanoribbon (GNR), a promising material that holds much potential for the future nanoelectronic devices, is introduced as a new material to overcome the limitation that exists in the conventional MOSFET. In this research, the analytical model of the GNR Schottky diode was presented to analyse the behaviour of metal-GNR interface. The work presents a simple model to analyse the current-voltage characteristic in the function of Schottky barrier properties such as the potential barrier and the Schottky barrier lowering effect of GNR contact. By using the analytical method, the analytical model for depletion region width, potential barrier, Schottky barrier lowering effect and the current-voltage characteristics of the GNR Schottky diode were presented. Besides that, the device structure of the GNR Schottky diode was built using Atomic Toolkit Virtual Nano Lab software to analyse the edge effect of metal-GNR interface. Based on the results, it is found that the potential barrier of GNR contacts is lower than conventional silicon contacts by at least half of it and the metal-Zigzag GNR interface shows promising potential to become interconnect as the interface is able to carry high current density up to $10^9$ A/cm$^2$. In addition, the proposed current-voltage characteristics model of GNR Schottky diode shows good agreement with experimental data and also with ATK Tools Simulation result.

# ABSTRAK

Permintaan tinggi terhadap saiz kecil, penggunaan kuasa yang rendah dan kelajuan pemprosesan yang tinggi merupakan faktor utama dalam pembangunan transistor. Bagi memenuhi permintaan terhadap transistor, trend semasa memerlukan saiz *Metal Oxide Semiconductor Field Effect Transistor* (MOSFET) dikurangkan kerana saiz transistor memainkan peranan penting dalam prestasi transistor. Walau bagaimanapun, mengurangkan saiz transistor secara ekstrem membawa cabaran-cabaran baru ke atas MOSFET yang menghampiri had prestasinya. Oleh itu, *Graphene Nanoribbon* (GNR) suatu bahan yang berpotensi untuk masa hadapan peranti nanoelektronik diperkenalkan untuk mengatasi kelemahan yang wujud pada MOSFET konvensional. Dalam penyelidikan ini, model analisis bagi diod Schottky dibentangkan untuk menganalisa hubung kait kelakuan logam-GNR. Penyelidikan tersebut membentangkan model yang mudah bagi menganalisis ciri arus-voltan berhubungan dengan ciri-ciri halangan Schottky seperti halangan keupayaan dan kesan pengurangan halangan Schottky bagi permukaan logam-GNR. Dengan menggunakan kaedah analisis, model analisis untuk lebar kawasan susut, halangan keupayaan, kesan pengurangan halangan Schottky dan ciri arus-voltan bagi GNR Schottky diod turut dibentangkan. Di samping itu , struktur peranti bagi GNR Schottky diod turut dibina dengan menggunakan perisian *Atomic Toolkit Virtual Nano Lab* bagi menganalisa kesan peminggiran permukaan logam-GNR. Berdasarkan keputusan, didapati bahawa halangan keupayaan bagi kontak GNR adalah lebih rendah daripada kontak silikon konvensional sebanyak separuh daripadanya dan permukaan logam-*Zigzag* GNR menunjukkan potensi cerah sebagai antara sambungan kerana ia mampu membawa arus ketumpatan yang tinggi sehingga $10^9$ A/cm$^2$. Selain itu, model ciri-ciri arus-voltan bagi diod Schottky GNR juga menunjukkan hubungan yang serupa dengan data eksperimen dan juga hasil Simulasi ATK Tools.

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# LIST OF SYMBOLS

| | | |
|---|---|---|
| $l$ | – | length of contact |
| $w$ | – | width of GNR |
| $n$ | – | number of dimer lines |
| $m$ | – | integer |
| $\xi$ | – | electric field |
| $\xi_j$ | – | junction electric field |
| L | – | depletion region width |
| $\varepsilon$ | – | permittivity of medium |
| $\varepsilon_G$ | – | permittivity of GNR |
| $Q$ | – | space charge volume density |
| E-k | – | Energy Dispersion |
| $a_{cc}$ | – | Lattice Constant |
| t | – | Tight Bonding Energy |
| k | – | Wave Vector |
| $\beta$ | – | Beta |
| p | – | Subband Index |
| $E_{gap}$ | – | Energy Gap |
| E | – | Energy |
| $n$ | – | Carrier Concentration |
| f(E) | – | Fermi Function |
| $E_F$ | – | Fermi Level |
| $k_B$ | – | Boltzmann's Constant |
| T | – | Temperature |
| $\Im_i$ | – | Fermi Dirac Integral |
| $h$ | – | Plank's Constant |
| $p^*$ | – | Momentum of Carrier |

| | | |
|---|---|---|
| q | – | Single Charge |
| η | – | normalized Fermi energy |
| $k_e$ | – | Coulomb's constant |
| $r$ | – | distance between the charges |
| $\xi_{MAX}$ | – | maximum electric field across the junction |
| $\Im_i$ | – | Fermi Dirac integral |
| $V_{bi}$ | – | potential barrier |
| $\Delta\phi$ | – | Schottky barrier lowering effect |
| $x$ | – | position of the maximum barrier |
| $\psi$ | – | potential |
| $J$ | – | current density |
| $J_{TE}$ | – | thermionic current density |
| $J_{TN}$ | – | tunnelling current density |
| $\varepsilon_o$ | – | Permittivity of Free Space |
| $V_a$ | – | applied voltage |
| $J_{sT}$ | – | reverse-saturation current density |
| $A^*$ | – | effective Richardson constant for thermionic emission |
| $V_{th}$ | – | Thermal Velocity |
| m* | – | Effective Mass of Carrier |
| $\alpha$ | – | Fitting Parameter |
| $V_i$ | – | intrinsic velocity |
| $\Theta$ | – | tunnelling probability |
| $A$ | – | area of metal-GNR contact |
| $I$ | – | current characteristic |

# LIST OF ABBREVIATIONS

| | | |
|---|---|---|
| FinFET | - | Fin-Field Effect-Transistor |
| MOSFET | - | Metal-Oxide-Semiconductor Field-Effect-Transistor |
| ITRS | - | International Technology Roadmap Semiconductor |
| CNT | - | Carbon Nanotube |
| GNR | - | Graphene Nanoribbon |
| I-V | - | Current versus Voltage |
| MATLAB | - | Matrix Laboratory |
| ATK | - | Atomistix Toolkit |
| ZGNR | - | Zigzag GNR |
| AGNR | - | Armchair GNR |
| DOS | - | Density of State |
| DFT | - | Density Functional Theory |
| WKB | - | Wentzel-Kramers-Brillouin |

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# CHAPTER 1

# INTRODUCTION

## 1.1 Background

The famous prediction known as Moore's Law states that the number of transistors in a die will be doubled every 18 months. This prediction was started of by Gordon Moore, one of the co-founders of Intel, in the year 1965 and his prediction is still true until today. It is the high demand of small sized, low power consumption and higher processing speed transistors that has prolonged the life of Moore's Law, and until now Moore's Law is still used as the guideline for transistor manufacturing. The Moore's Law graph is shown in Figure 1.1.

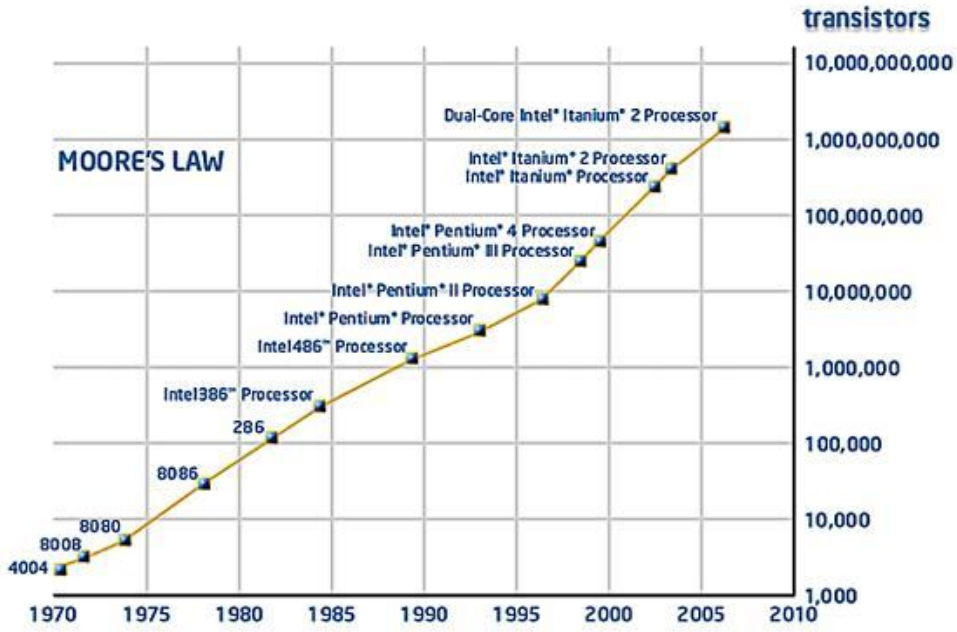


**Figure 1.1:** Moore's Law graph [1]

In order to fulfill the Moore's Law, the size of the transistor needs to be scaled down drastically. However extreme scaling down of the size of the transistor will brings more harms than benefits. Further downsizing the transistor, especially the channel length, has a lot of limitations which severely affect the expected performance of the devices. The transistor is expected to reach its channel length limits before year 2020 [2]. Conventional methods of scaling the size of a transistor do not offer the best solution to further prolonging Moore's Law. Therefore, scientists have come out with two different solutions. One is to develop the transistor using a totally new structure, and another is to implement new materials to replace current silicon technology.

Today the idea of using new structure to build a transistor has been implemented in the semiconductor industry. The first new-structured-transistor used in the semiconductor industry was released by Intel in the year 2011, with the release of its Ivy Bridge (microarchitecture) processor based on tri-gate (3D) transistor, or commonly known as Fin-Field-Effect-Transistor (FinFet). Due to this major improvement on the development of the transistor, Moore's Law can be further prolonged for a few more years. However, this 3D structure transistor will reach its limit sooner or later. The last resort to continue prolonging Moore's Law is to depend on the second solution, which is using new materials to replace silicon.

The most promising material which many scientists believe can replace the current silicon technology is graphene [3]. This new material has a two-dimensional honeycomb lattice structure demonstrates very intriguing properties, such as high electron mobility at room temperature [4]. High electron mobility is desired in electronic device because high mobility is able to produce higher output. Currently, no graphene based device is being produced on an industrial scale but intense study on the material has been underway for many years. It is believed that the first graphene based device will be available within a decade.

To fully implement graphene based devices on an industrial scale, a prototype of the graphene based device needs to be built and tested many times. However building a device using new materials with many uncertainties is very expensive and time consuming. Due to these problems, modeling and simulation come in handy to study the characteristics of the graphene based device before it is fabricated and undergoes final testing.

Table 1.1 shows the modeling and simulation challenges of Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) for gate channel size around 14nm listed by International Technology Roadmap Semiconductor (ITRS). ITRS is a set of documents produced by a group of semiconductor industry experts from five leading chip manufacturing regions in the world. These experts are representative of the sponsoring organisations which include the Semiconductor Industry Associations of the US, Europe, Japan, South Korea and Taiwan. ITRS predicted that novel materials and devices will replace the CMOS technology before silicon based technology reach its limit in the year 2020.

**Table 1.1:** Modeling and Simulation Difficult Challenges [5]

| **MOSFET $L_{ch} \geq 14nm$** | **MOSFET $L_{ch} < 14nm$** |
|---|---|
| 1. Lithography simulation including EUV | 1. Modeling of chemical, thermomechanical and electrical properties of new materials |
| 2. Front-end process modelling for nanometer structures | 2. Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials |
| 3. Integrated modeling of equipment, materials, feature scale processes and influences on devices and circuit performance and reliability, including random and systematic variability | 3. Optoelectronics modeling |
| 4. Nanoscale device simulation capability: Methods, models and algorithms | 4. NGL simulation |
| 5. Electrical-thermal-mechanical-modeling for interconnect and packaging | |
| 6. Circuit element and system modelling for high frequency (up to 300GHz) applications | |

## 1.2 Problem Statement

The introduction of graphene has led to intensive studies being conducted on graphene based transistors such as carbon nanotube (CNT) field-effect transistors or graphene nanoribbon (GNR) field-effect transistors. These graphene based transistors are believed to be the future of nanoelectronic devices and could replace the current silicon transistor technology [3]. However people tend to forget that the roots of the technology evolution toward a transistor are based in an understanding and

development of diode action. Thus it is important to study the behaviour of graphene based diodes first because the study of graphene based diodes can be the building block on which production of graphene based transistors will be developed.

Currently the graphene based diodes proposed by many researchers are carbon nanotube Schottky diodes [6] and graphene nanoribbon Schottky diodes [7]. The GNR Schottky diode is the focus of this research. The GNR Schottky diode is a Schottky diode that involves a metal-GNR contact. GNR is used for the semiconductor region of the GNR Schottky diode and the metal terminal for the GNR Schottky diode is usually high work function metal such as palladium or gold [8].

Due to the high mobility of graphene, the proposed GNR Schottky diode is said to have better performance in terms of its current characteristics. However GNR is a new material and many questions still remain unanswered, such as how it behaves when in contact with metal.

Many questions have arisen on the Schottky barrier properties, such as how the depletion region width and build-in potential barrier will behave in the metal-GNR contacts. Also how the Schottky barrier effects such as Schottky barrier lowering effect affects the performance of GNR Schottky diode when a voltage is applied across it. A further question is how the Schottky barrier properties affect the I-V characteristic of a GNR Schottky diode. Such questions are still left unanswered.

## 1.3 Research Objective

The focus of this research is to model the Schottky barrier properties and I-V characteristics of GNR based Schottky diode. The following are the objectives of this research:

1. Study and analyse the depletion region width, potential barrier and Schottky barrier lowering effect of metal-GNR contacts.

2. Model the I-V characteristic of GNR based Schottky barrier diode.

3. Evaluate the performance of GNR based Schottky diode by comparing the developed I-V model with experimental data.

## 1.4 Research Scope

In order to achieve the objectives mentioned in Section 1.3, the research is conducted based on the following scopes:

1. Model the depletion region width, potential barrier and lowering Schottky barrier effect of one-dimensional monolayer GNR based Schottky barrier.

2. Model the I-V characteristic of monolayer GNR based Schottky barrier.

3. Simulate the model developed using MATLAB software.

4. Validate the developed I-V model with Atomistix ToolKit (ATK) Tools Simulation.

## 1.5 Contributions

The Schottky barrier diode is a diode that is made up from metal-semiconductor contacts. Metal-semiconductor contacts are a fundamental physical parameter that exists in almost every semiconductor device. Currently most of the electronic devices in an integrated circuit are connected by means of metal-semiconductor contacts. Moreover, all integrated circuits communicate with the rest of the electrical system via metal-semiconductor contacts. Thus, research on graphene based Schottky diodes is very useful in the application of electronic components.

Currently, Schottky diodes are an electronic component that is widely used for radio frequency applications, as well as being used in power application as a rectifier. Additionally, Schottky diodes are used in a variety of applications, such as photodetector, solar cell, microwave mixer and various integrated circuits. They play an important role in various semiconductor applications.

The purpose of this research is to investigate the metal-semiconducting GNR contacts. By conducting this research, a better understanding of the behaviour of metal-semiconducting GNR is obtained. This is important because the quality of the metal-semiconducting GNR contacts plays an important role in the performance of various semiconductor devices and integrated circuits. Therefore this research can be the basic guideline for predicting the characteristics of metal-semiconducting GNRs.

## 1.6 Outline of Thesis

The research aims is to analyse the metal-semiconducting GNR contacts and develop the GNR Schottky diode model. There are 6 chapters in this thesis. The first chapter discusses on the background study, problem statement, objectives, scopes and contributions of the research. The literature review regarding the basic theory of graphene, GNR and Schottky diode was performed in Chapter 2. It provides the fundamental principle behind the research. Besides that, discussion on the previous studies regarding metal-graphene material interface was also presented in Chapter 2.

In Chapter 3, the research methodology, including the research activities, research flowchart and modeling flowchart were discussed. The software tools used to undergo the research were also reported in Chapter 3. The modeling of the fundamental parameters such as Schottky barrier properties of GNR contacts was demonstrated in Chapter 4. The modeling part in Chapter 4 includes the modeling of depletion region width, potential barrier and Schottky barrier lowering effect.

The current-voltage characteristics of the GNR Schottky diode as well as the performance evaluation were discussed in Chapter 5. In addition, the edge effect on the metal-GNR interface was also discussed in Chapter 5 by using the ATK Tools Simulation software. Finally Chapter 6 discusses the conclusion of the research and proposal for future work.

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